WP2: Multiprocessors communication networks for PetaFLOPS supercomputers

1. Main activities and results

Task 2.1: ***System Area Network Topology Design: network simulation and communication performance evaluation.*** A comparative analysis of the SAN's communication performance parameters has been made on the basis of simulation experiments considering the most popular network topologies for interconnecting thousands of nodes such as K-ary n-cube, 3D Torus, High Radix Clos Network, Fat Tree, Flattened Butterfly and TOFU. The outcome is that High Radix Clos Network and its modifications are the most promising solutions as well as the combination of Fat Tree hierarchical crossbar architecture. An architectural design of a high speed switch has been suggested. The communication performance parameters of the suggested switch architecture have been evaluated on the basis of simulation experiments varying the packet size, the traffic type and the switch radix. We have investigated and analyzed multicore processors architectures such as Tile64 и PicoArray and on the basis of profound comparative analysis we have selected an embedded multicore processor for implementing the core of the suggested switch architecture thus ensuring low latency and high bandwidth, especially for streaming multimedia and graphic applications. As a result of the activities involving WP2 up to now IBM Blade Center has been installed at "High Performance Computing and GRID Technology" lab, Computer Systems Dept., Technical University of Sofia, hardware platform based on Blade Server HS22, 2xXeon Quad Core E5504 80w 2.00GHz/800MHz/4MB L2, 3x2GB and 3 high performance Blade severs, HS21, Xeon Quad Core E5405 80w 2.00GHz/1333MHz/12MB L2, 2x1GB Chk, O/Bay SAS, disk subsystem IBM System Storage DS3400 Single Controller and hard disk for disk subsystem IBM 750GB Dual Port HS SATA HDD, Blade Center, IBM eServer BladeCenter(tm) H Chassis and record device 2x2900W PSU UltraSlim, chassis switch for Blade Center, BNT Layer 2/3 Copper Gb Ethernet Switch Module, optical switch for chassis Blade Center, Brocade(R) 10-port 4 Gb SAN Switch Module with optical switch IBM Short Wave SFP Module, adequate cabling, NetBAY S2 42U Standard Rack Cabinet and power supply Ultra Density Enterprise C19/C13 PDU Module (WW). The platform is used for simulation and communication performance evaluation of the suggested switch architecture and SAN architecture.

The team, responsible for the tasks of WP2, has acquired knowledge and skills to use the software environment of the "IBM Blade Center" at the "High Performance Computing and GRID Technology" lab, Computer Systems Dept., Technical University of Sofia.

High speed XR switch architecture with cut-through routing of the "wormhole type" has been designed with extra port for the host. The switch has a modular structure (Fig.1). The dynamic communication parameters of the switch have been evaluated experimentally on the basis of simulation by utilizing the discrete event simulator OMNeT++. Four types of spatial traffic patterns are simulated and analyzed for 2D Mesh network with "DOR" routing algorithm: uniform, bit-reversal, transpose and complement. Generated traffic (or arrival rate) in this simulation was exponentially distributed function, representing homogenous Poisson process.

The results obtained show that for the case of uniform network traffic latency increases more slowly as the offered load increases. The network bandwidth is highest for the case of uniform network traffic. For complimentary-type of traffic and DOR routing the capacity of the communication channels in X direction are loaded maximally before the flits of the packet take the turn in Y direction. For matrix transpose and bit-reversal traffics the communication performance deteriorates as a result of the high probability for traversing the same communication channels.

We have evaluated and analyzed the dynamic communication parameters of the suggested high speed switch XR of radix 8x8 and the SAN of 2D Mesh topology built upon it (array of NxN XR switches) on the basis of simulation experiments in the OMNeT++ environment. The simulation experiments have been conducted for 3 case studies of the packets distribution in the traffic: uniform, Gauss and exponential, varying the mesh size (4x4, 8x8 и 16x16) and each host generating 2000 packets of size 50 flits (Fig.5)

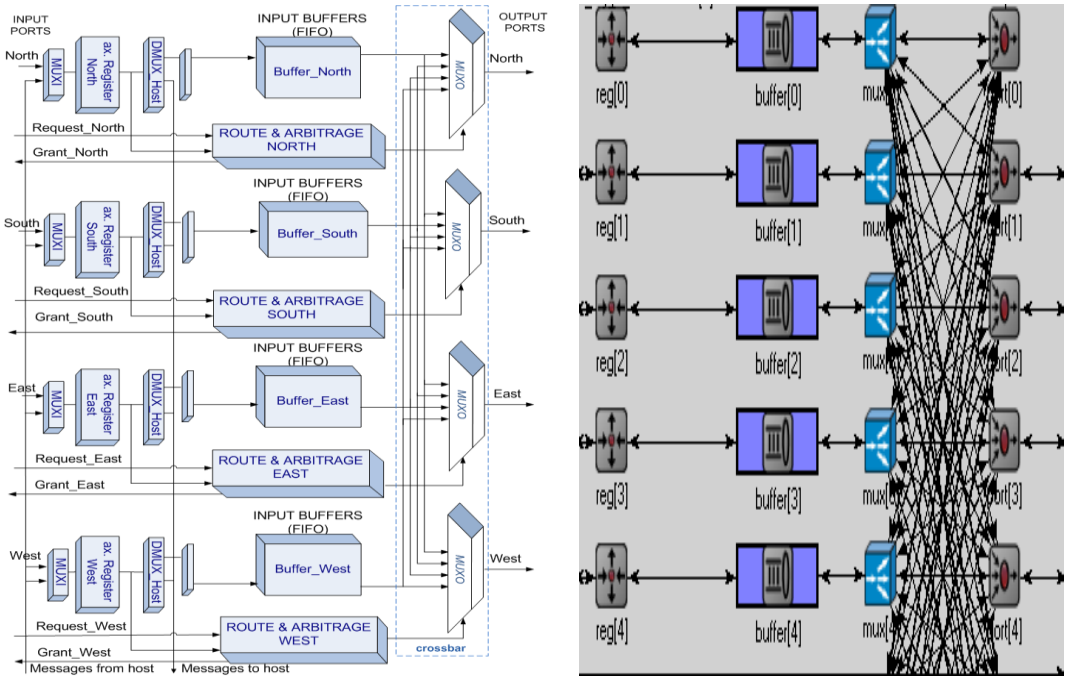


Fig 1. Architectural design of the high speed switch XR.

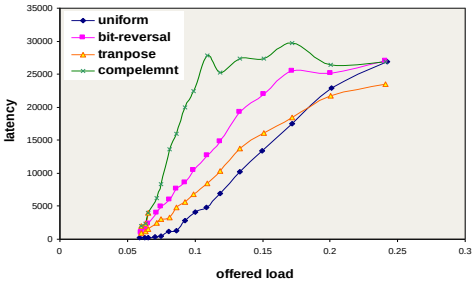


Fig. 2: Network latency for various types of traffics

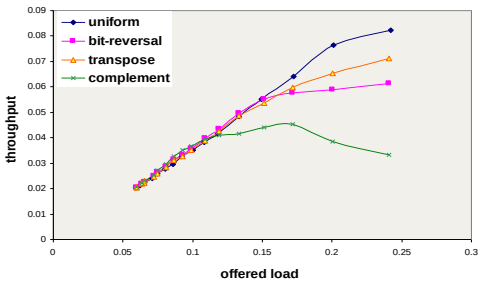
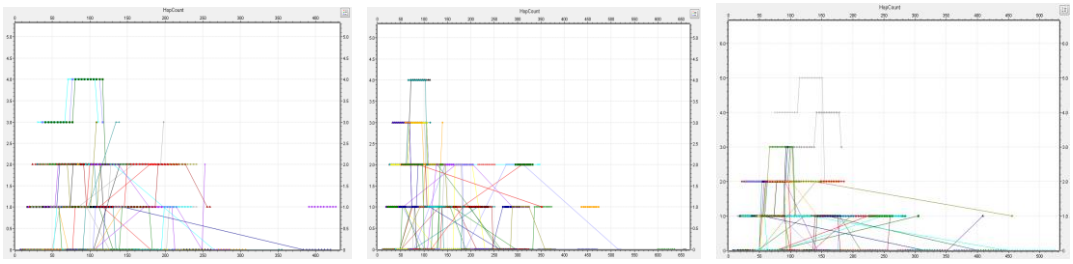


Fig.3: Network bandwidth for various types of traffics



(1) (2) (3)

Fig. 4: Hop count) for mesh size 4x4
(1) uniform traffic; (2) Gauss traffic; (3) exponential traffic

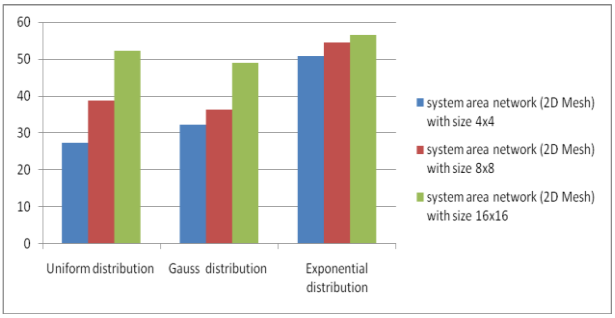


Fig. 5: Network latency (2D Mesh) varying the size 4x4, 8x8, 16x16

The dynamic performance parameters of YARC switch have been evaluated and analyzed on the basis of simulation experiments for the case studies of uniform and Gauss distribution network traffics. The motives for implementing YARC chips in the supercomputer SAN are their architectural adaptability to the limitations of modern ASIC technology – large number of links and limited number of buffers. The simulation experiments have been conducted in the OMNET++ environment. The YARC switch is modeled as an array of tiles. The components of the model are: DFlipFlop, SidebandExtractor, TileInputQueues, RoutingLogic, RowLines, RowBufferArray, ColumnLines, ColumnBufferArray, SidebandAdder.

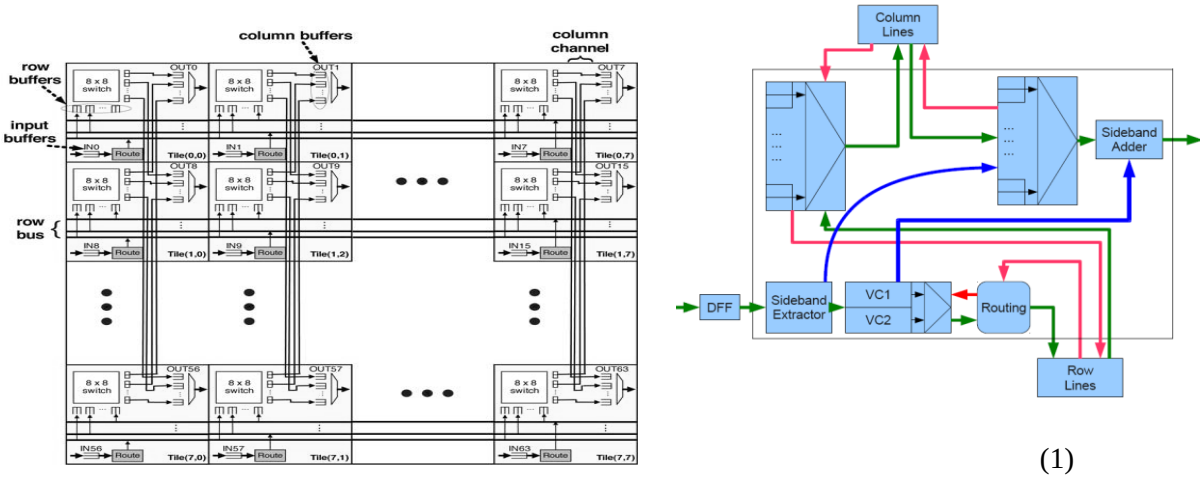


Fig. 6: YARC architecture (1) and its model in OMNET++ environment (2)

The green lines in Fig. 6.2 visualize the path of the flit; the red lines represent the internal start/stop signals. Simulation results show that latency is quite low for Gauss distribution traffic of 2000 packets of size 20 flits (Fig.7).

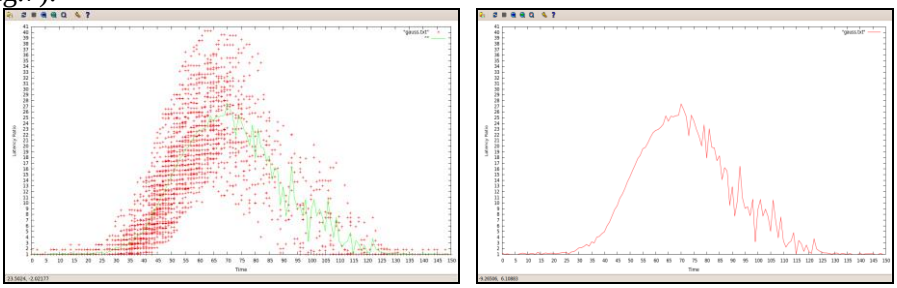


Fig. 7: Latency of YARC switch for Gauss distribution traffic (100% probability)

We have investigated latency of the YARC switch for uniform traffic of 100%, 50% and 30% probability, respectively. Results show linear latency increase versus time. For the case study of 50% probability latency increases more slowly (Fig. 9).

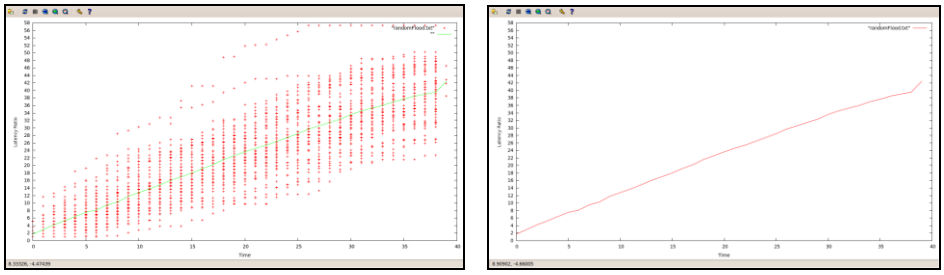


Fig. 8: Latency of YARC for uniform traffic
(100% probability)

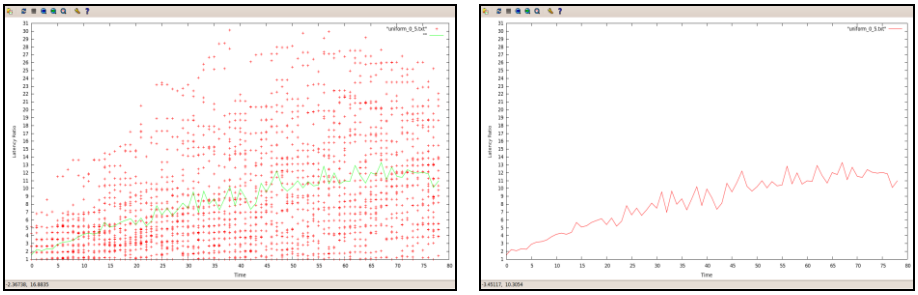


Fig. 9: Latency of YARC for uniform traffic
(50% probability)

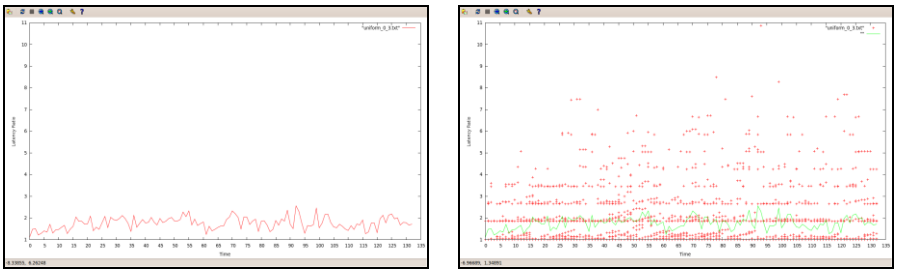


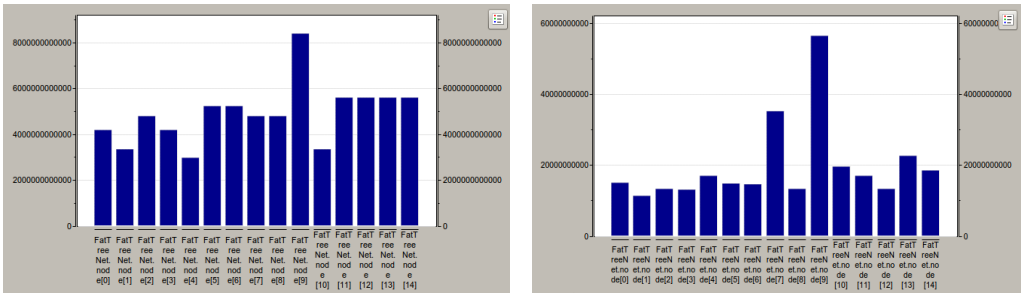
Fig. 10: Latency of YARC for uniform traffic
(30% probability)

The SAN dynamic performance parameters of Fat Tree topology implemented with YARC chips have been estimated and analyzed on the basis of simulation experiments in the Omnet++ environment. The routing algorithm is based on routing tables that are filled in initializing the network and are not subjected to changes afterwards. The routing directions are associated with specified ports: Up – port 0, port 1, port 2; Left – port 2, port 3, port 4; Right – port 5, port 6, and port 7. The dynamic communication performance parameters for collective personalized exchange (Gossiping) and Ping-pong traffic of 2000 messages are shown in fig.11. Obviously, the communication parameters for the case study of Gossiping outperform the parameters for Ping-pong traffic.

We have evaluated and analyzed the dynamic communication performance parameters of the suggested XR switch of radix 16x16. The scalability of the XR switch gives the opportunity to build up large scale SAN's with a wide spectrum of routing algorithms. The simulation model of the XR switch (Omnet++ - based) is shown in Fig.12 and comprises the modules: inRegister; Queue; outPort; HostArbiter; Clock. The synchronization of the modules is implemented on the level of Request/Grant messages. Simulation experiments have been conducted for the case studies of traffics of uniform, Gauss and exponential packet distribution, total number of packets 2000, and 256 flits packet size.

For uniform distribution each packet has a random destination in the range 0-16, by avoiding sending packets from the host to itself. Latency results of release are in the range 6-32ms except for PortH. This is due to its unbuffered input. Port loading is obtained as a result of the number of sent packets separated time simulation (Packets/ms). The parameters of Gaussian distribution is (8, 1.5) and of exponential distribution is (8, 0.66). The number of packets is predetermined - 2000. In the Gaussian and exponential distribution ports are loaded unevenly. Therefore, the total execution time is significantly greater (2 times).

Additionally the dynamic characteristics of the extended high-speed switch design 32x32 are investigated and analyzed (Fig.14). The result analysis shows, the highest throughput and the lowest latency of the switch design are achieved for the case of Gauss network traffic.



(1) (2)

Fig. 11: Histograms with the throughput values for collective personalized exchange (Gossiping) (1) and Ping-pong (2) traffic pattern of 2000 messages

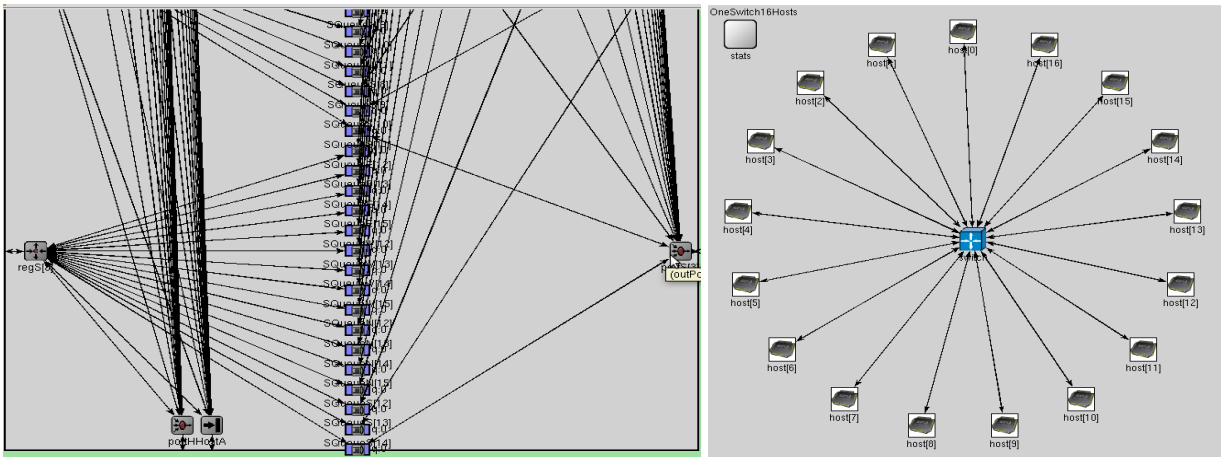
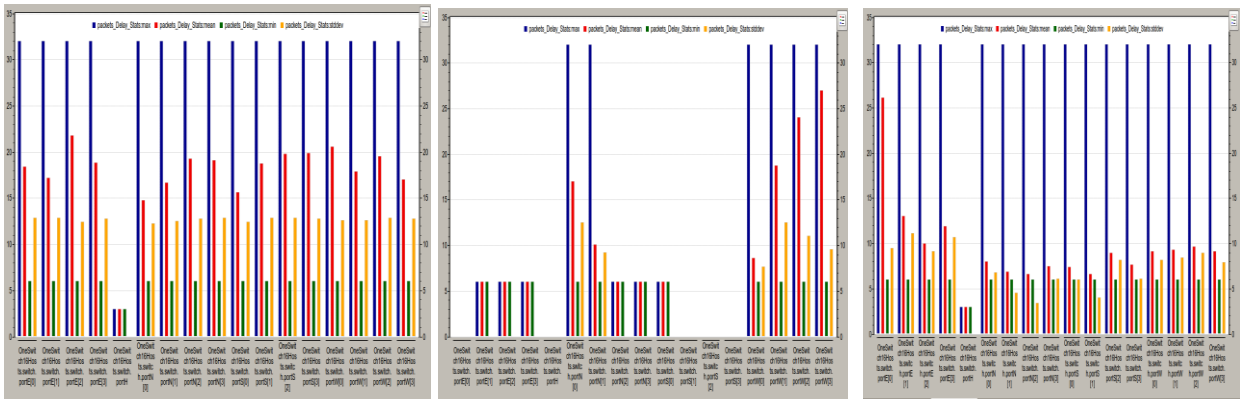


Fig. 12: a) Ned file of switch with radix 16x16; b) Network.ned - 1 switch 16+1 host (Stats module) to display the results



a) Uniform traffic pattern
Avg latency per port: 15.6959
Total time: 248375

b) Gauss traffic pattern
Avg latency per port: 7.4535
Total time: 494102

c) Exponential traffic pattern
Avg latency per port: 8.4780
Total time: 443813

Fig. 13: Latency per port – max, mean, min, stddev

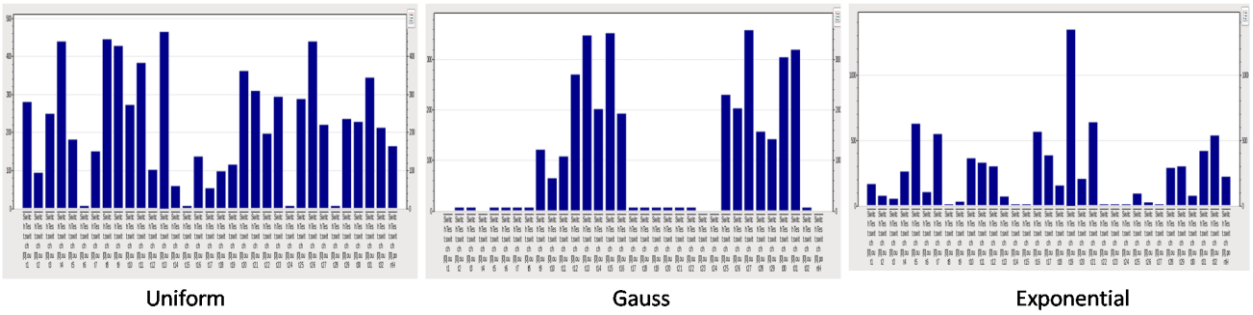


Fig. 14: Average latency of XR switch with radix 32x32

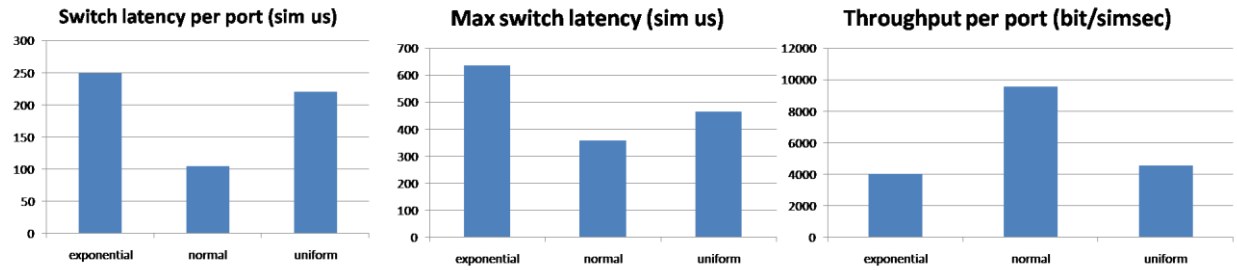


Fig. 15: Communication performance parameters of XR switch with radix XR 32x32

From the collected results until now and the analysis it can be concluded, that the proposed architectural design of high-speed switch with radix 4x4, and its extensions – switches with radixes 8x8, 16x16 and 32x32 show good dynamic characteristics for various traffic patterns and can be used as a component in developing system area network designs for supercomputers.

The dynamic characteristics of TOFU (6D Mesh/Torus) network are analyzed. The analysis has been performed for the case of uniform and "gossip" network traffic pattern with packet size of 32 and 64 flits and packet counts 100000.

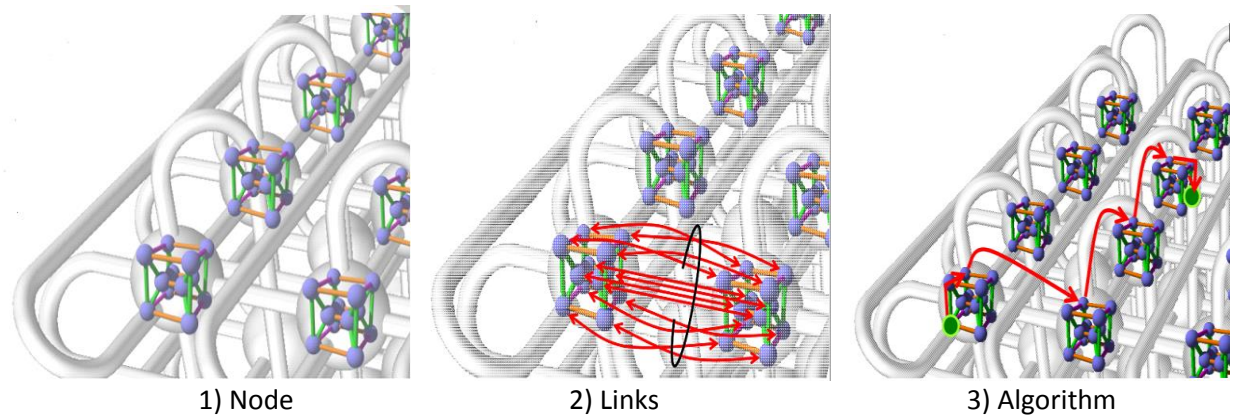


Fig. 16: TOFU system area network

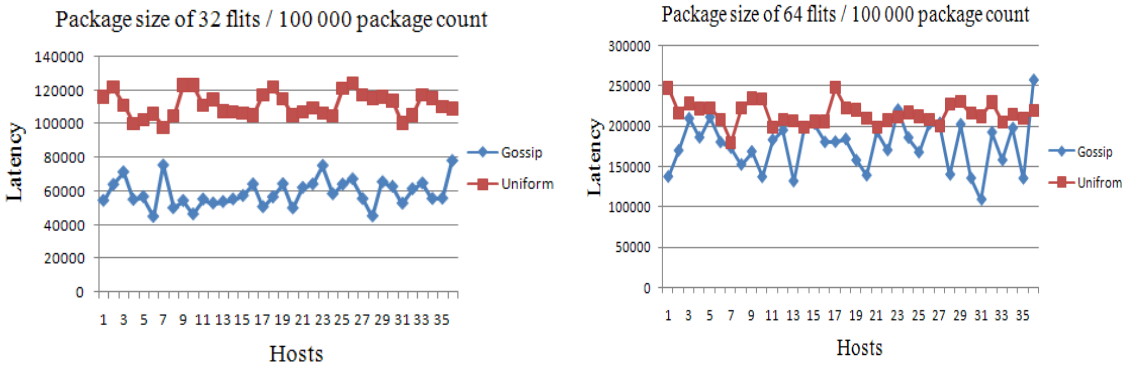


Fig. 17: Latency per port

The gathered results of the simulation experiments (Fig. 17) show lower latency, when collective personalized exchange "gossip' is used, compared to the normal packet distribution in the network, which is caused by the fact, that in "gossip" the messages are being sent from each node to all other nodes. The count of the destinations, accessible over a minimal hop count is very big. In this way, most of the latencies are very small and the overall latency has lower value.

With respect to the performance of the system area networks, there is need for developing a new architectural design of communication network, which has to satisfy the requirements of the high performance computer systems and to ensure low latency and high throughput.

The hierarchical structure of "αΩ HIGHWAY" system area network is proposed on two levels: level Omega and level Alpha. The Omega level consists of a multiring intracluster highway, which provides alternative routes in case of communication resources failure using network flow recirculation. The Omega level is based on a multi-stage communication network with a cyclic structure and does not contain single points of failure. The computer cluster is divided in S cluster segments. The multiring intracluster Omega highway ensures the link between the cluster segments (inter-segment link). It is assembled via XR (eXtended Radix) switches. Each of them is directly connected to the cluster segment, for which the switch provides input and output links to the intracluster highway. The communication between the computing nodes in each cluster segment is implemented from the level for intersegment communication, Alpha. The Alpha level embeds switches with YARC architecture (Matrixes of crossbar switches).

The topology of the multiring intracluster highway Omega is based on the topology of multi-stage Omega network. A network, created using concatenation of Omega network and reverse Omega network (mirrored) is non-blocking, at the expense of adding new stages. In order to increase the reliability of the network and to ensure fault tolerance of the communication resources, a cyclic structure is created, in which the first and the last stage of the non-blocking Omega overlap. At least one input port and one output port are added to each switch of the cyclic Omega, for connection to specific segment of the computer cluster. In this way, the output indirect Omega network is transformed in a direct cyclic Omega network. At the place of the host is a cluster segment connected via a YARC switch.

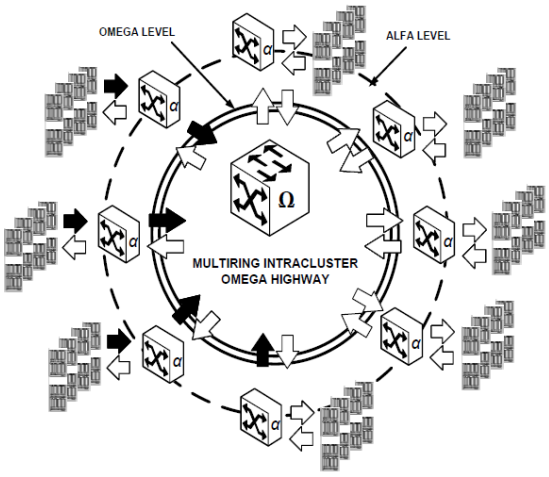


Fig. 18: "αΩ Highway" system area network architecture

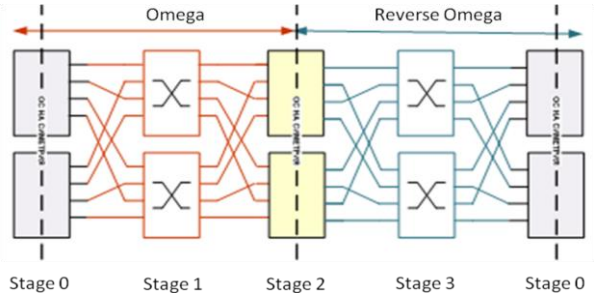


Fig. 19: Concatenating of Omega and Reverse Omega Network

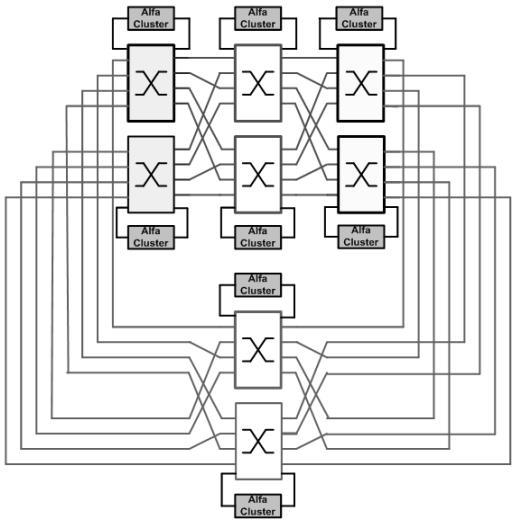


Fig. 20: "ΩHighway" Network with Alfa sub-clusters intra-connected

Simulation models of the multiring network and the XR switch are developed, using the OMNET++ IDE. The dynamic communication parameters of the proposed system network architecture are evaluated based on simulation experiments (Fig.22). The results of this task are submitted in [BK_12s].

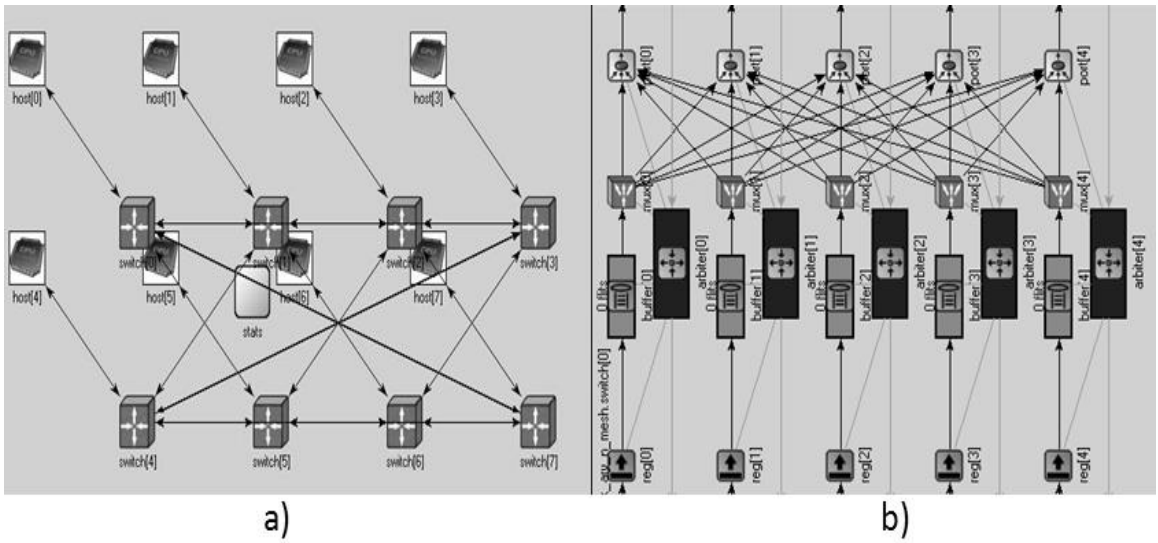


Fig. 21: Simulation OMNET models
a) Omega network; б) XR switch design

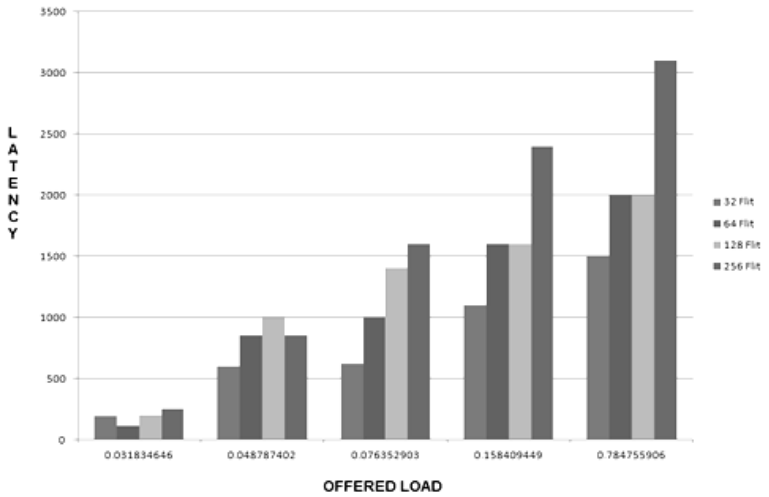


Fig. 22: Latency vs. offered load

The proposed new Grand Clos architectural design is a hybrid design of Fat Tree and Clos, named Grand Clos. As a hybrid model, it has significant advantages, compared to the classic Clos and Fat Tree topologies. Actually, the new topology design consists of multiple interconnects of the Clos topology, connected in a Fat Tree network. The most important part of the topology is the horizontal links between the nodes of the fat tree on the same level. They minimize the needed hop count in order to communicate from one level to another. Also, these horizontal links reduce the load of the root node. Normally, it splits the Fat Tree network in two parts. Therefore, the entire traffic from the first part to the second one has to go through the root node. In our design the horizontal links help with the communication between the parts of the network, which leads to increased throughput and minimized latency. In addition, the link between the closses is reliable, because every node has connection to the others, based on a Crossbar. So, our idea is to use the advantages of both topologies in the best way in a hybrid model, with additional improvement – horizontal links. This will decrease the network latency, which is seen from the simulation results. The results of this task are submitted in [I_13, BI_13].

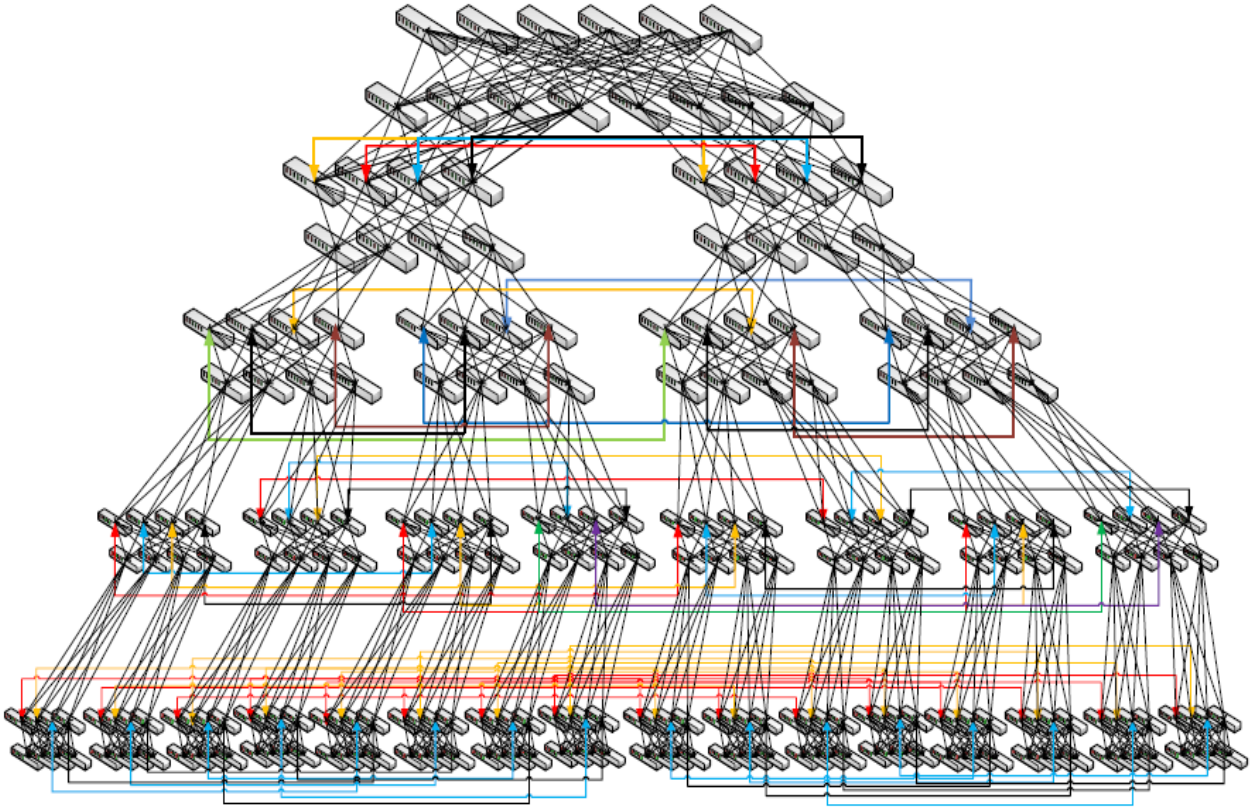


Fig. 23: System area network for collective communication “Grand-Clos”

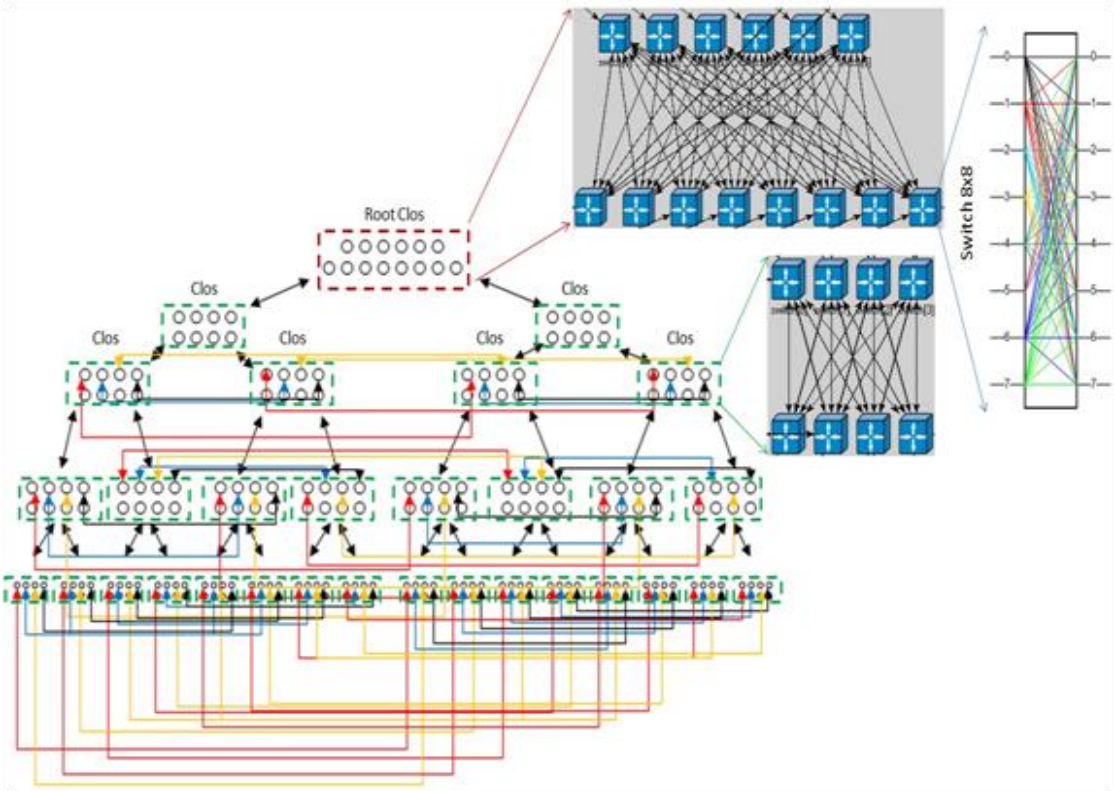


Fig. 24: “Grand Clos” system area network topology

In order to show the advantages of the proposed Grand-Clos architectural design, the simulations are compared with a regular Fat Tree network under the same conditions (packet size, traffic pattern and total packets transmitted). The results from all simulations, provided in Fig.12, show that our Grand Clos Network achieves around 15% lower latency in all simulations. This performance increase explains the usage of the horizontal links in the proposed new network design of Grand Clos topology.

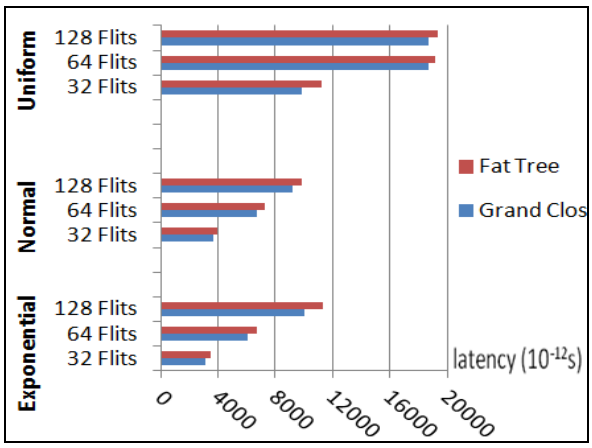


Fig. 25: Simulation results of Grand-Clos and Fat Tree Networks

During the last months of the project, meetings with WP1 team are organized. Discussed are the tasks, set in the corresponding WPs and the possibilities for their implementation and realization. The regular meetings of the team responsible for WP2 at the Technical University of Sofia are organized, with the discussions, powerful presentation according to WP tasks and comments on the obtained results. The results on this task are published in [NBKA_09], [BNL_09], [BNIRM_09], [BIIG_09], [BGG_09], [BGGM_09], [NBAS_10], [BNIIG_10], [BNGG_10], [BNMIF_11], [BGM_11], [BGMGA_11], [BIIG_11], [BIIMA_11], [BNIGI_11], [BNGGM_11], [BNGG_11], [BI_11], [BA_11], [BK_12], [BIF_12], [BK_12], [I_13], [BI_13].

Task 2.2: FPGA network realization. Functional and architectural design of a switch design with radix 4x4 (with 4 input and 4 output ports) is performed, of information packets, which can be exchanged over high-speed serial channels between computers in a multi-computer system with parallel architecture (cluster). For this purpose is used WebPACK, an IDE for automated design and the high-level language VHDL for input switch description. The switch is designed as a multi-core system with shared RAM for input and output packet queues. With the help of the IDE the switch is implemented on a programmable field-programmable gate array (FPGA chip). As main implementation's parameters are the following reported:

1) The percentage of used resources by the integrated circuit (the freed resources can be used for future expansion of the switch.

2) The latency of the signals in the switch, from which its speed and throughput can be estimated. With logical check of its function in mind, an RTL – level (Register Transfer Level) simulation is performed on the implemented switch with the help of the ModelSIM simulator. The results of the performed examinations of the feature of the FPGA chips' architecture are presented in 2 publications, reported on the International Scientific Conference "Computer Science'09". These results are used for design, simulation and implementation on a FPGA chip, [MD_09], [K_09], [MN_11].

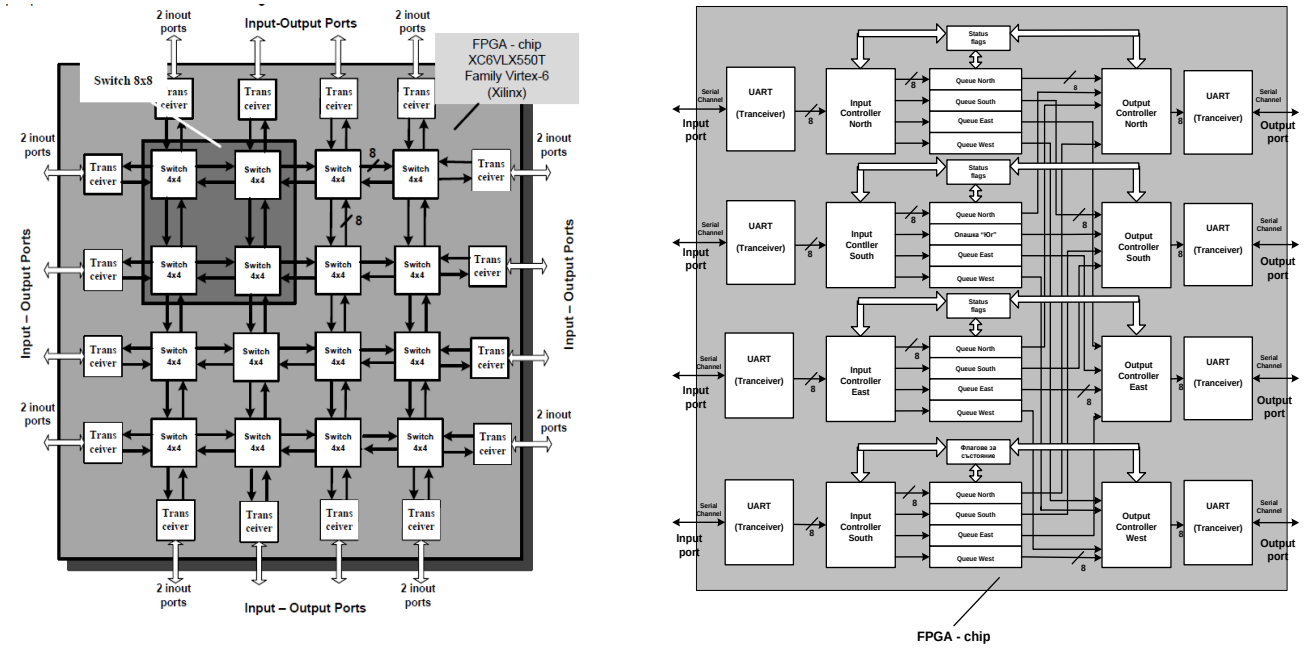


Fig. 26: Switch design with radix 32x32, implemented on FPGA chip (Virtex6, Xilinx)

Designed, implemented on FPGA and investigated are two types of router architectures for high-speed system area networks. The approaches, used in the router architecture design, are fundamentally different:

1) The first architecture is based on dual port RAM memory and dedicated input and output controllers for every input and output port. Controllers are implemented as programmable CPUs, which run in parallel. Routing decision is made by the firmware running in the input controllers.

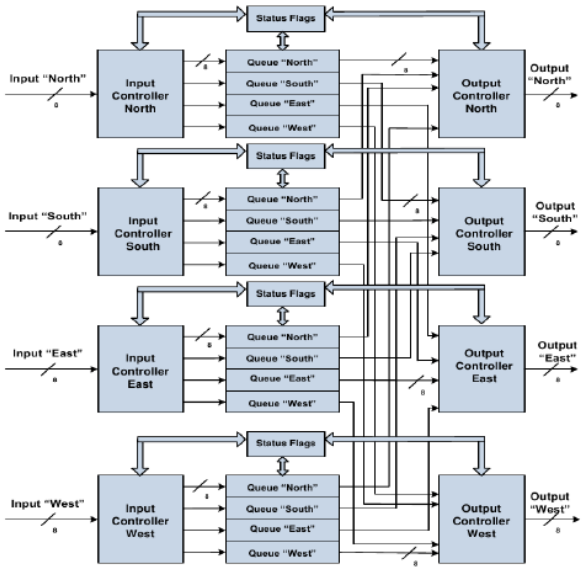


Fig. 27: Router Architecture with parallel controllers and firmware control

2) The second router architecture is built around a crossbar and dedicated input controllers for every input port. Crossbar configuration is done by a single output controller. Both input controllers and output controller are implemented as finite state

machines. Routing decision is made by additional module which provides fast lookup based on TCAM memory.

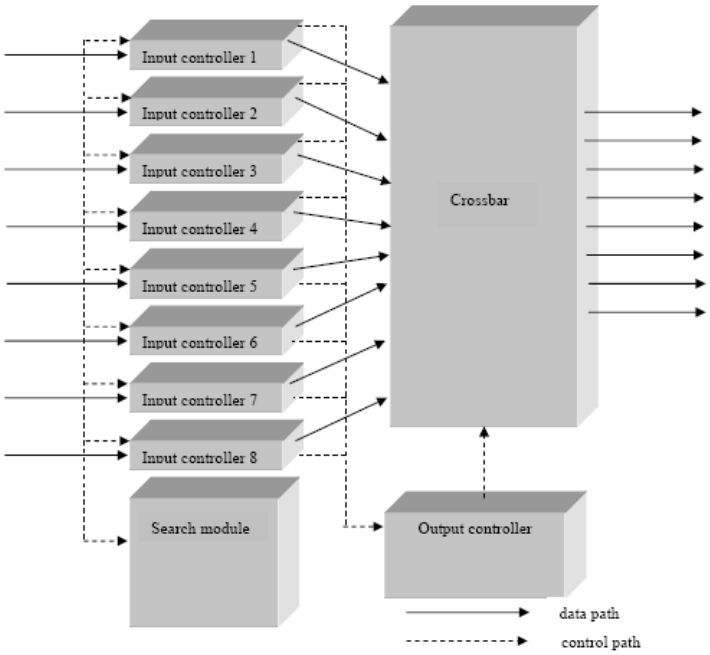


Fig. 28: Router Architecture with Crossbar and hardware control

Using Xilinx ISE WebPACK as Integrated Development Envionment (IDE) , the designed two types of router architectures are implemented on FPGA of Xilinx Virtex 6 family (XC6vlx75). The derived by IDE parameters, as the percentage of used FPGA -resources , the maximum clock frequency and the router signal delays are used to estimate the FPGA-implementation. Router simulation models are created and the simulation of the router architectures in pipeline mode is realized by Omnet++ simulator. Using simulation results, the speed and throughput of router architectures are estimated.
The used FPGA development boards are connected to computers by serial interfaces and form a computer stand to examine and test the FPGA router functioning.

Fig. 29: A part of computer stand for FPGA router examinaion

The results of the performed router architecture design and examination are presented in 3 publications, reported on: the XI International Scientific Conference “ELECTRONICA 2012”, the XXI International Scientific Conference “Electronics – ET2012”, the XI International Conference “Challenges in Higher Education and Research in the 21th Century”.

2. Publications with acknowledgments to the project DCVP 02/1

a) published:

[NBKA_09] O. Nakov, P. Borovska, N. Kuchmova, D. Andreeva, Multiprocessor-based real-time control of a moving object, 8th WSEAS Int. Conf. on Applied Computer and Applied Computational Science (ACACOS '09), 20-22 May 2009, Zhejiang University of Technology, Hangzhou, China, Proceedings, 495-499

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3. Presentations and reports within the internal meeting held at the Technical University – Sofia

The project is carried out regular internal team meetings at the TU responsible for WP2 which are presented and discussed research activities and obtained results on following topics: system area networks, supercomputing architectures, topologies of networks system for supercomputers, switches and supercomputers and more.

4. Others

[1] Organizational and financing activities: Contract No:091-CH-001-09 from 10.06.2009г.

[2] Equipment purchase under WP2.

[3] Adaptation and supplement the educational content of the course in High-Performance Computer Systems, Parallel Programming course and Metaheuristics course at the Computer Systems Department, Technical University of Sofia (Plamenka Borovska, Desislava Ivanova).

[4] Additional activities for dissemination and popularization of the obtained results:

a) International scientific workshop "Supercomputer Architectures and Applications" and presentations within the Fifth International Conference "Computer Science' 2009" - 05-06.11.2009g. The conference is organized under the direct guidance and management of the Computer Systems Department at the Technical University – Sofia, prof. Borovska.

b) Participation in the scientific workshop "Supercomputing Architectures and Applications", 19-21.03.2010, Velingrad and paper presentation in the frame of the scientific workshop, organized by the "SuperCA++" project coordinator, Prof. St. Margenov.

c) Participation in the regional conference "Supercomputing Applications in Science and Industry", Sunny Beach, on 20-21.09.2011, organized by the project coordinator, Prof. St. Margenov.

d) Promotion of “SuperCA++” project in journal "COMPUTER & COMMUNICATIONS ENGINEERING", prof. Plamenka Borovska.

e) Promotion of “SuperCA++” project in journal "Automatics & Informatics", br.3/2011

f) Organization, management and execution of International scientific workshop "Supercomputer Architectures and Applications" and presentation of plenary papers presenting achieved project results within the Sixth International Conference "Computer Science'2011" - 01-03.09.2011g., Ohrid, Macedonia.

j) Promotion of “SuperCA++” project and the WP2 results in the frame of Happening: “Supercomputer Challenger” aims to promote high-performance computing at the secondary educational level and to attract pupils for active participation in the future HPC training activities and projects, 29.03.2012, Pravets, Bulgaria.

h) Promotion of “SuperCA++” project in the TV show "Career" on TV Europe Channel.

i) Promotion of “SuperCA++” project in broadcasting "To the top" on DARIK radio.