WP1: High Performance Architectures towards PetaFLOPS based on Multi-Core Processors

1. Main Activities and Results

Task 1.1: The Node Architecture of the PetaFLOPS supercomputer. According to the activities defined in task 1.1. a preliminary node architecture of the supercomputer is designed. The number of processors, the memory structure and hierarchy, cache memory structure, some improvement of the coherent protocols in multiprocessor environment with shared memory and distributed caches, and introduction of processing resources in main memory are described.

Large number of computer simulations is performed using both available simulators for computer architectures and our own programs, designed for specialized simulations of different computer architectures. The results received during the experiments are described in: a paper entitled "PIM – Memory Modules with increased Performance and Intelligence" published in the Journal "Information Technologies and Control", a presentation entitled "Analytic Evaluation of Heterogeneous Shared-memory Multiprocessors" on the International Conference "Automatics and Informatics'09" in Sofia 2009, and a report entitled "Research of System Characteristics and Parameters for Multithreading Processors through Simulation", prepared for presentation on a scientific event. The results in the task are achieved with the participation of Vladimir Lazarov, Maria Marinova, Todor Tashev and Svetoslav Tashev.

Task 1.2: The Tree architecture of PetaFlops supercomputer. In order to realize the activities of the task the main efforts were concentrated in the definition of the optimal structure for networking the different nodes of the supercomputer, oriented to different tree architectures. During the research we analyzed the influence of the different structures on the global throughput and bandwidth and the mutual possible blockages between the nodes. Special attention was dedicated on the problem of latency in long distance accesses to information. The analyses are performed analytically and through computer simulations.

The results in this task are presented in a paper entitled "Implementation of a Parallel Architecture for Radix-2 FFT", published in the Journal "Information Technologies and Control". The results in the task are achieved with the participation of Vladimir Lazarov, Maria Marinova and Julia Zidarova.

2. Publications, connected to the project with citation of DO 02-115/08

a) published:

[PCLZI_09] Ph. Philipov, I. Costov, V. Lazarov, Z. Zlatev, M. Ivanova. Implementation of a Parallel Architecture for Radix-2 FFT, Journal Information Technologies and Control, Year VI, Nr. 2 (2009), ISSN: 1312-2622, 12-16.

[LZPI_09] V. Lazarov, Z. Zlatev, Ph. Philipov M. Ivanova. Analytic Evaluation of Heterogeneous Shared-memory Multiprocessors, International Conference Automatics and Informatics"09, (2009), Proceedings, ISSN: 1313-1850, vol. I, 1-4.

[TTT_09] T. Tashev, S. Tashev, N. Tasheva. PIM – Memory Modules with increased Performance and Intelligence, Journal Information Technologies and Control, Year VII, Nr. 3 (2009), ISSN: 1312-2622, 17-22.

d) in preparation:

[LMMp] V. Lazarov, M Marinova, T. Marinov. System Characteristics and Parameters Evaluation for Multithreading Processors through Simulation.

3. Other activities

[1] Organizational activities: Periodical meetings of the Operational Committee. Creation of operational group for organizing the work in WP1, WP3 and WP4 (S. Margenov, K. Boyanov, V. Lazarov, K. Georgiev, I. Dimov).

[2] Purchasing of equipment for WP1 (V. Lazarov, M. Marinova, T. Tashev, S. Tashev, J. Zidarova).

[3] Configuring the working place for FPGA design and purchasing the necessary equipment (V. Lazarov, M. Marinova, T. Tashev, S. Tashev, J. Zidarova).

[4] Preparation of specifications and purchasing of necessary software products for WP1 (V. Lazarov, M. Marinova, T. Tashev, S. Tashev).

[5] Adaptation and enlargement of the content of course “High Performance Computer Architectures”, teach at Center for Education in BAS and NBU (V. Lazarov, M. Marinova). .